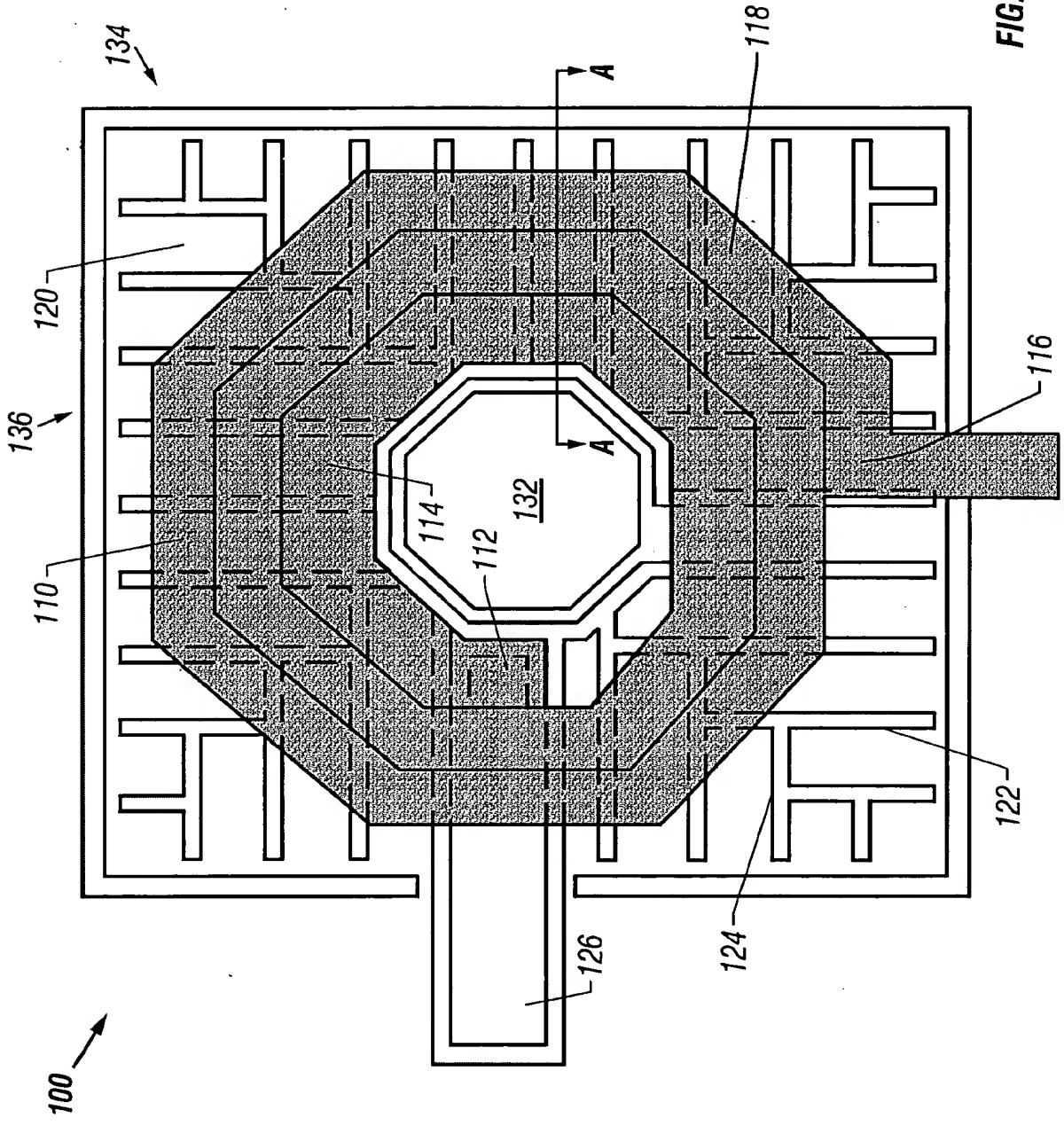


FIG. 1

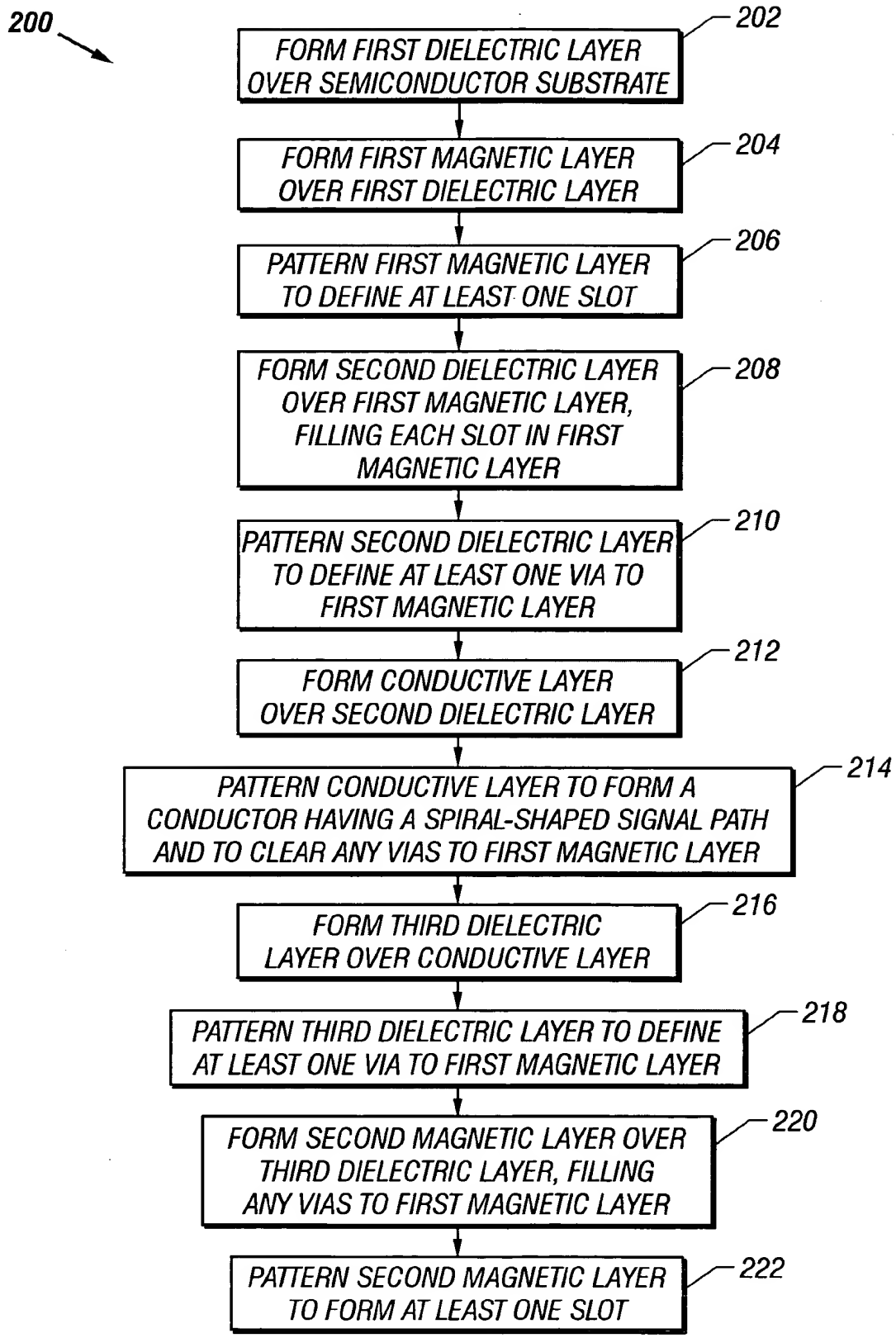


FIG. 2

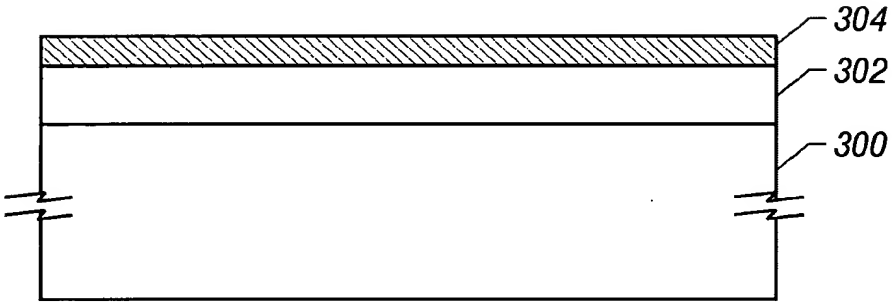


FIG. 3

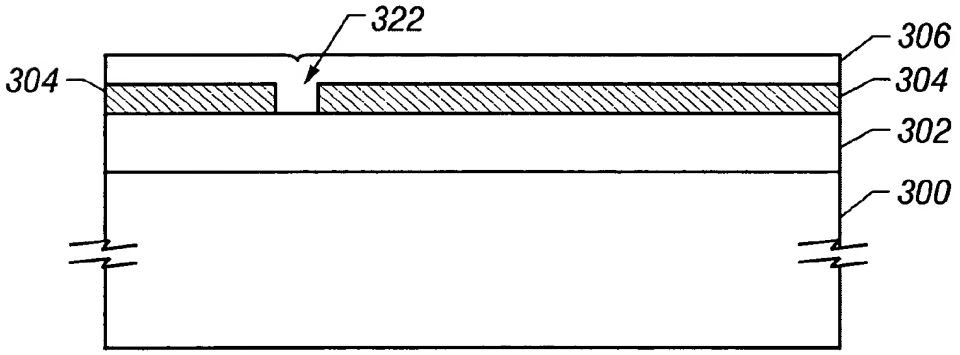


FIG. 4

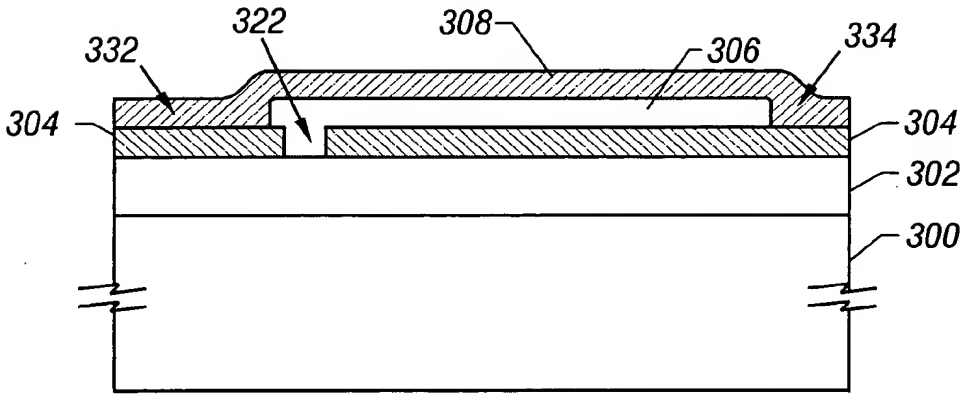

322
308
332
306
334
304
304
302
300

FIG. 5

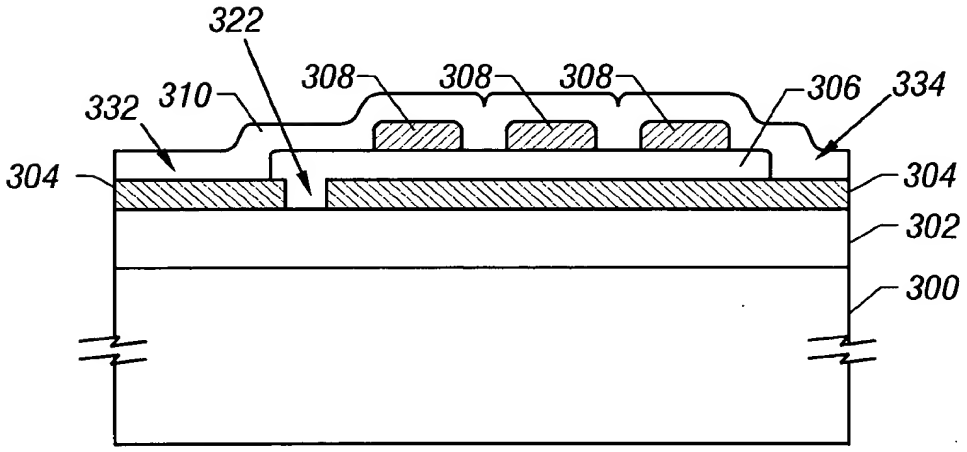

322
308
308
308
332
310
306
334
304
304
302
300

FIG. 6

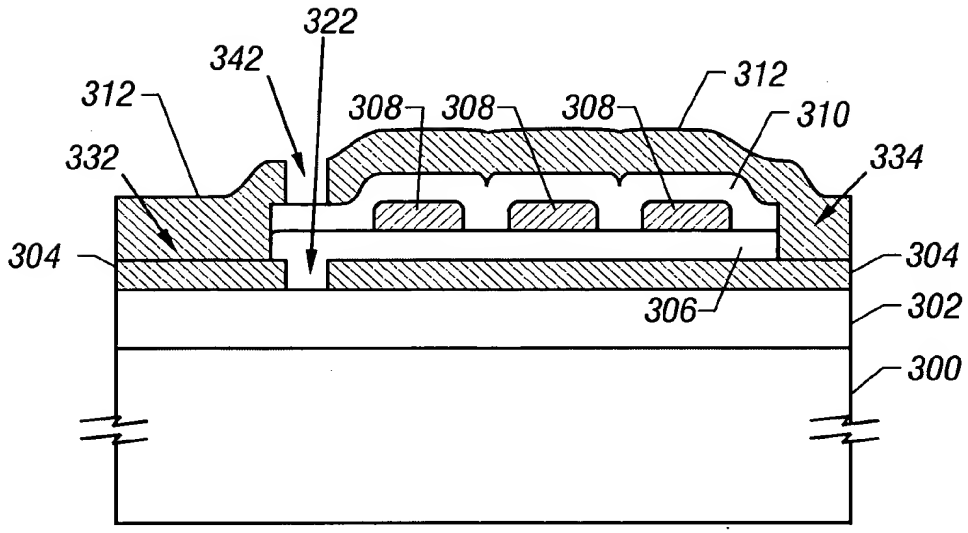

322
342
312
308
308
308
312
310
332
334
304
304
306
302
300

FIG. 7

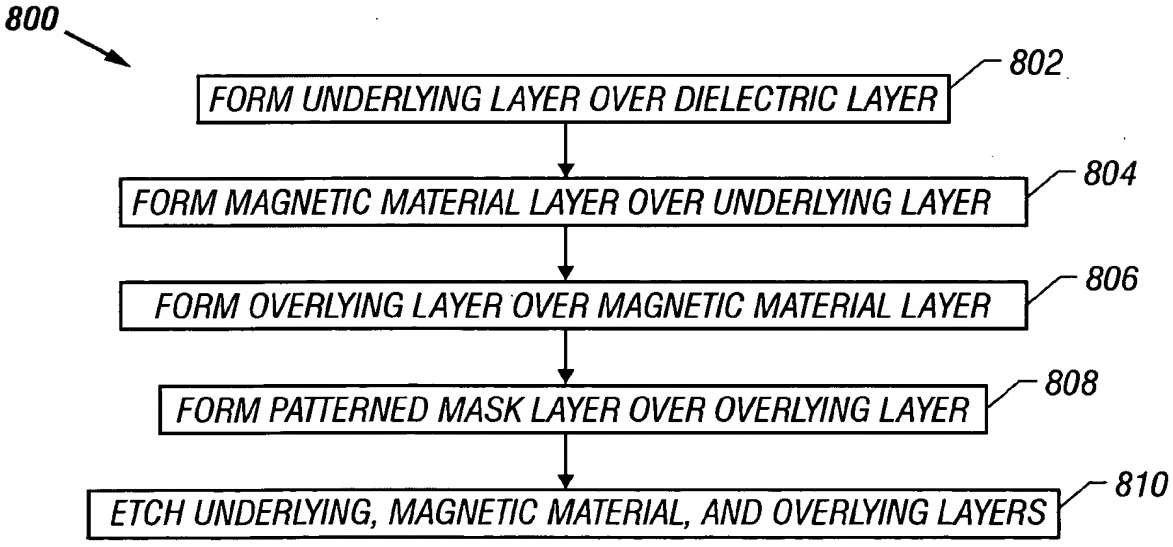

800
FORM UNDERLYING LAYER OVER DIELECTRIC LAYER
802
FORM MAGNETIC MATERIAL LAYER OVER UNDERLYING LAYER
804
FORM OVERLYING LAYER OVER MAGNETIC MATERIAL LAYER
806
FORM PATTERNED MASK LAYER OVER OVERLYING LAYER
808
ETCH UNDERLYING, MAGNETIC MATERIAL, AND OVERLYING LAYERS
810

FIG. 8

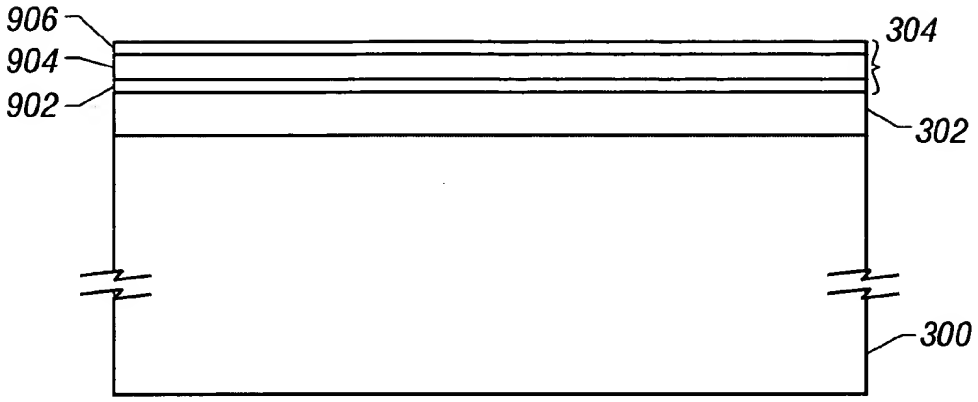


FIG. 9

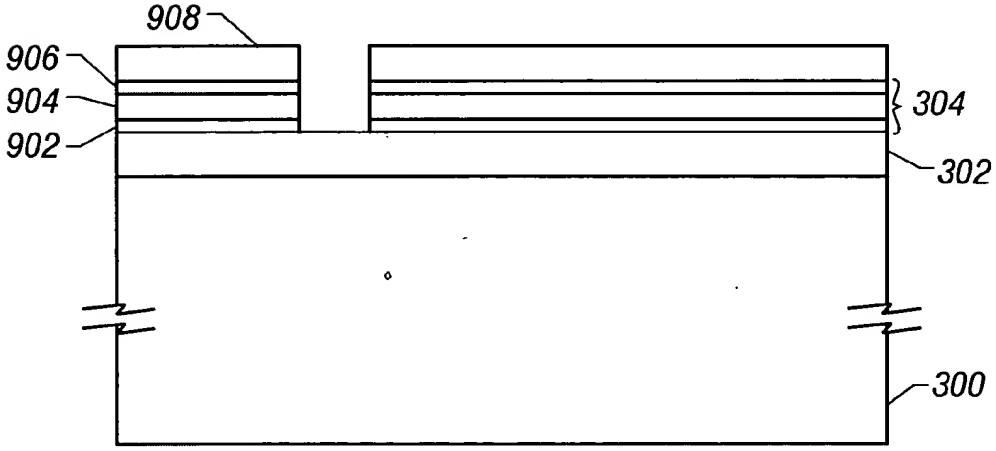


FIG. 10

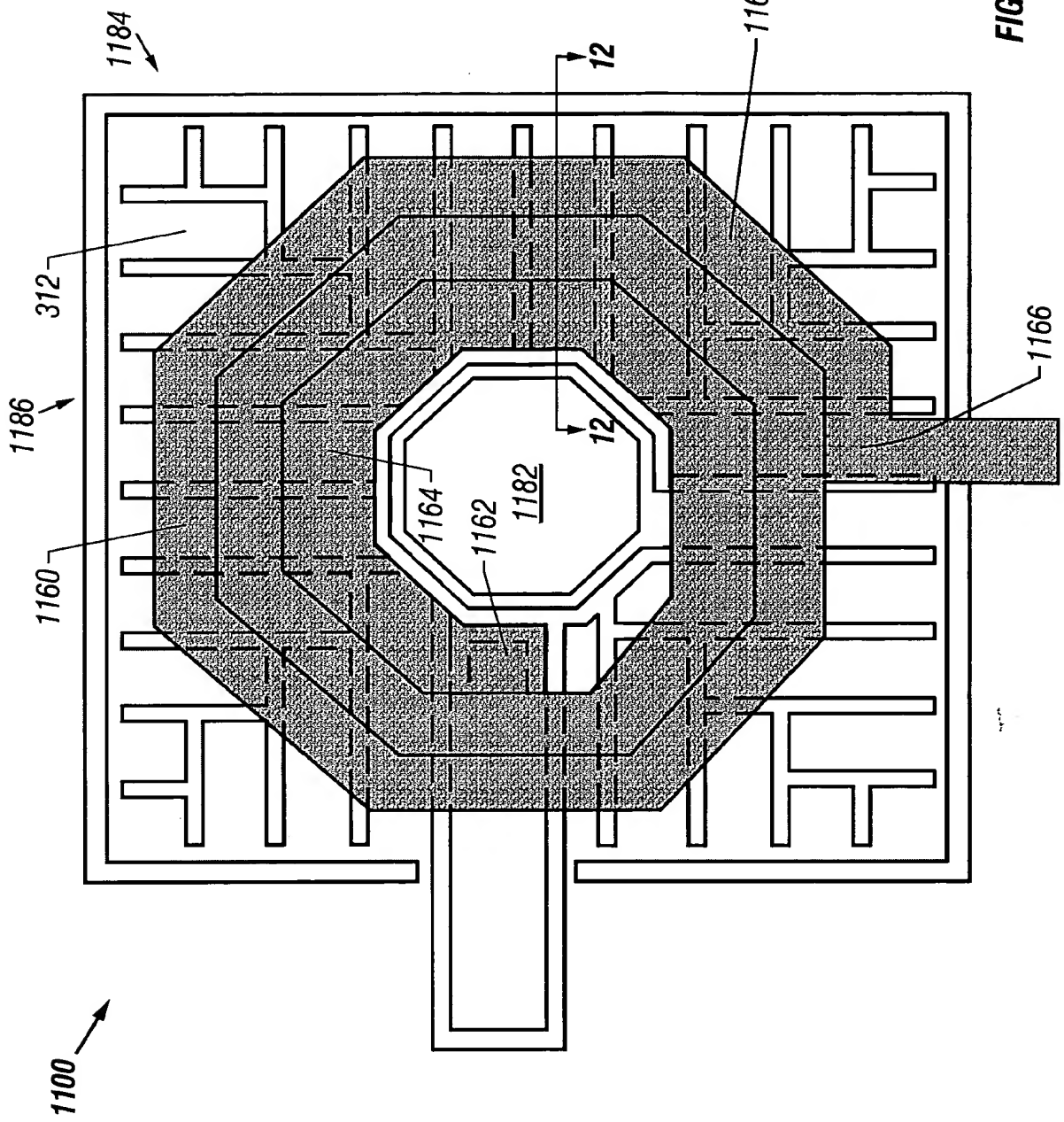


FIG. 11

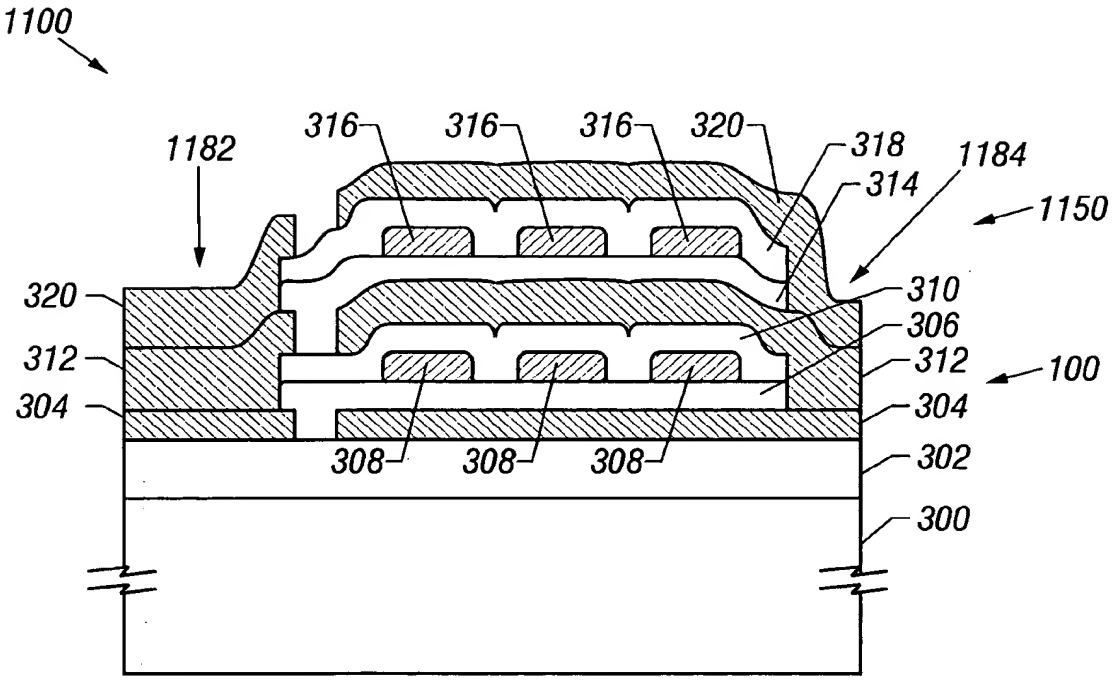

1100
1182
316
316
316
320
318
314
1184
1150
320
310
306
312
312
100
304
304
308
308
308
302
300

FIG. 12

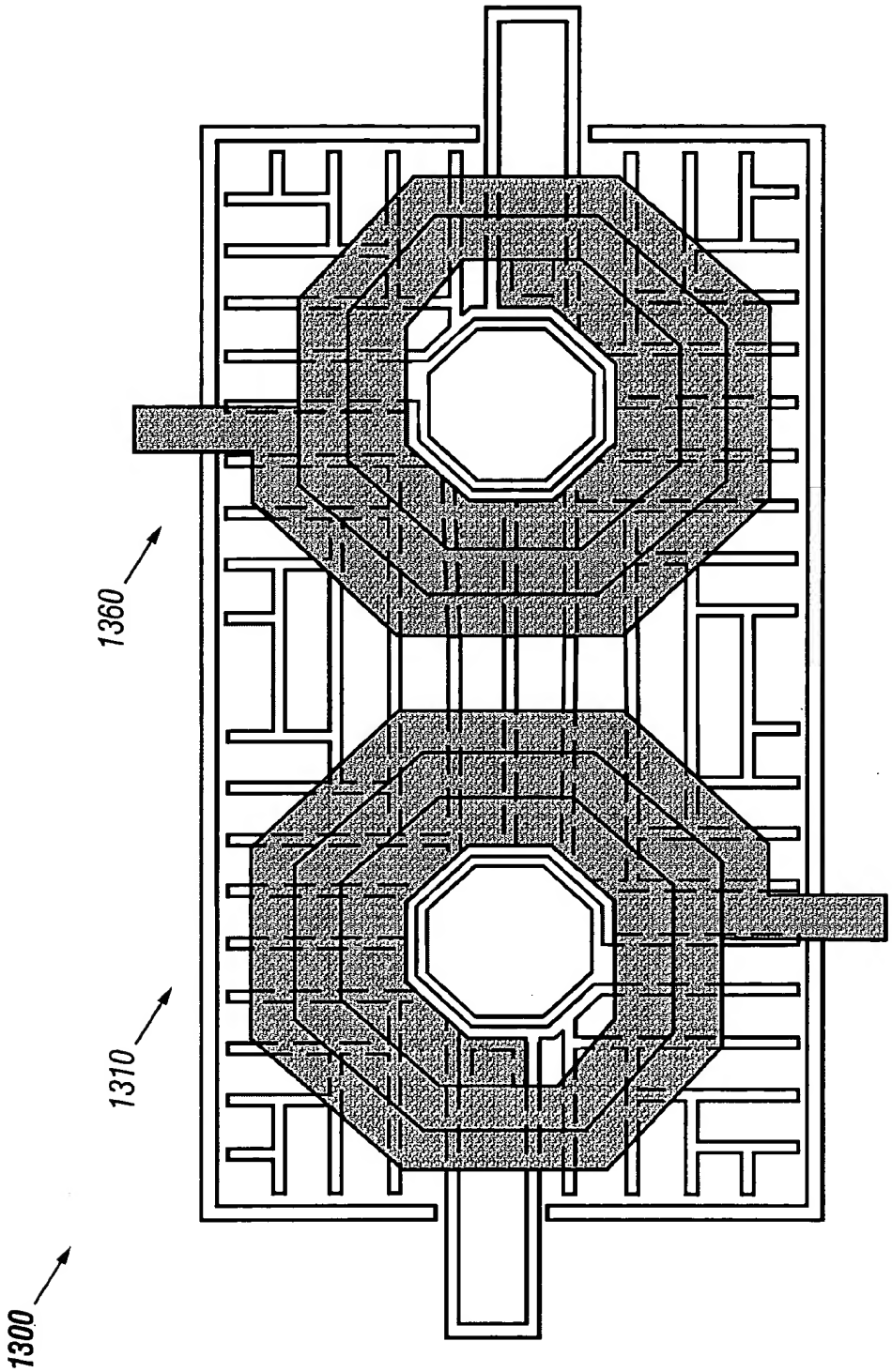


FIG. 13

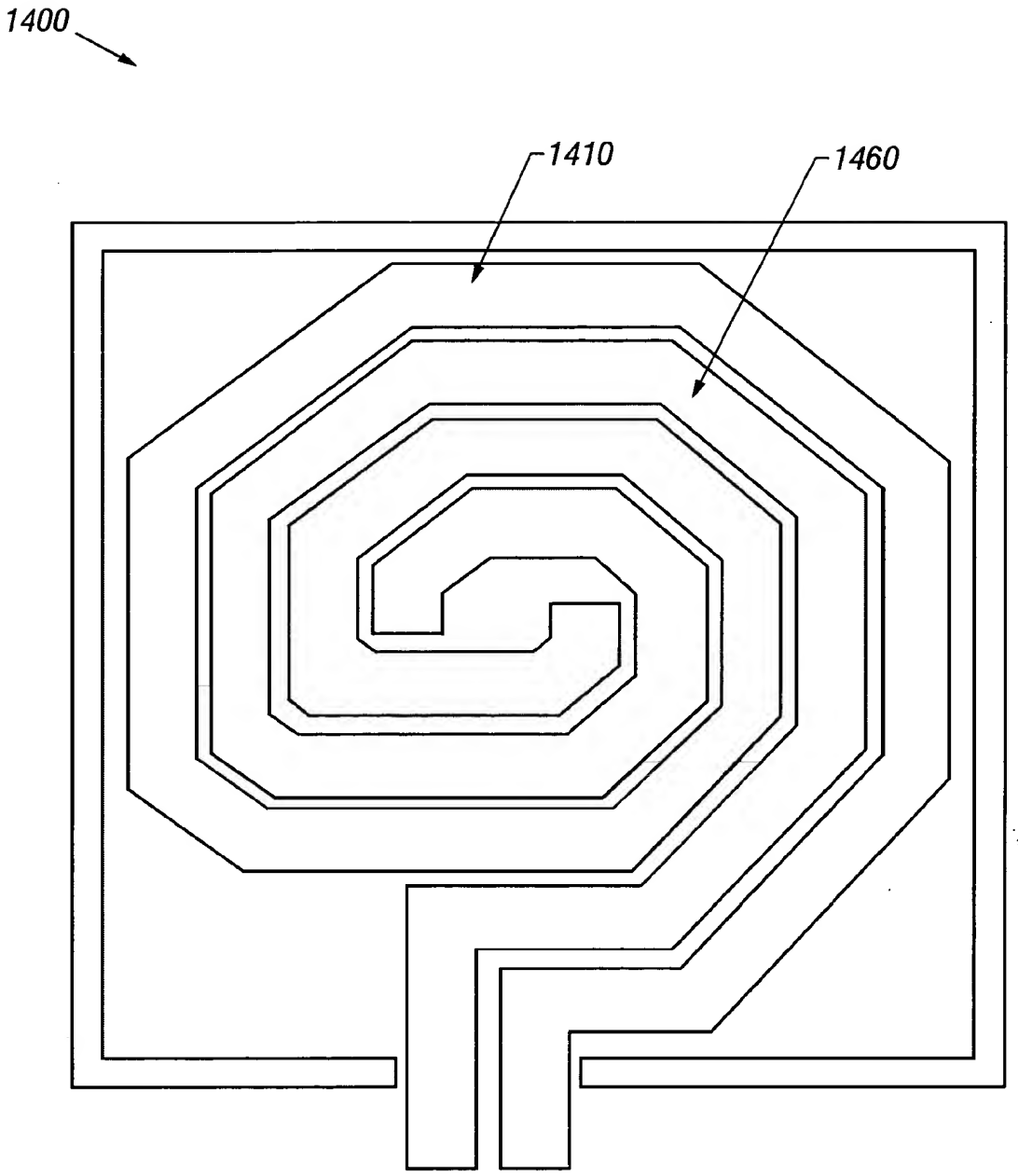


FIG. 14

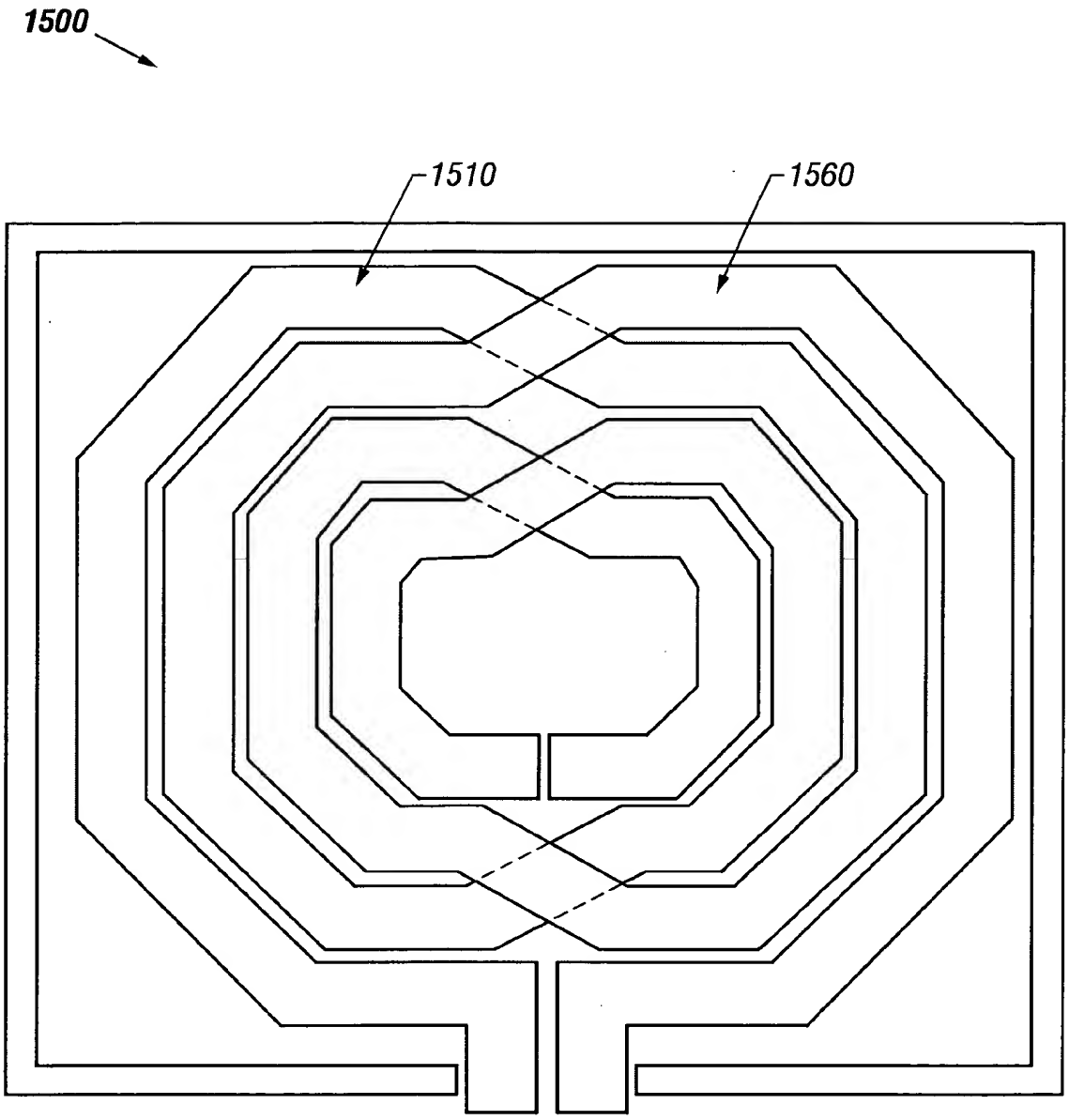
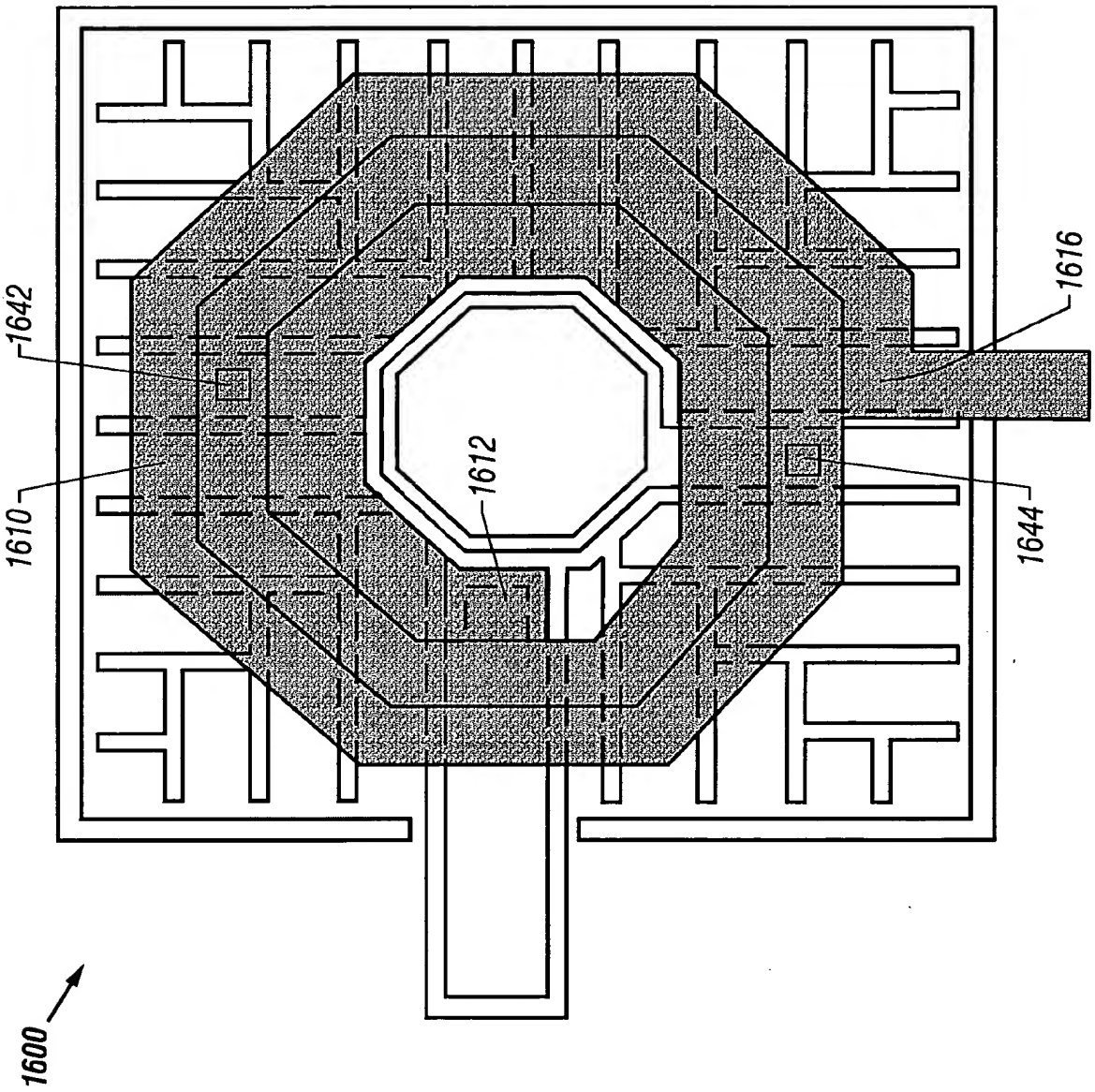


FIG. 15

FIG. 16



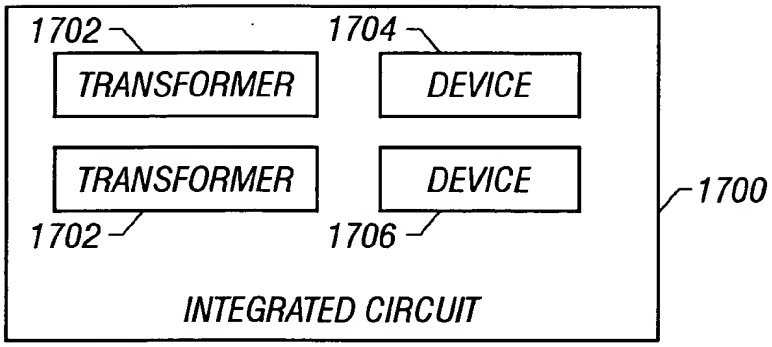

1702
1704
TRANSFORMER
DEVICE
TRANSFORMER
DEVICE
1700
1702
1706
INTEGRATED CIRCUIT

FIG. 17

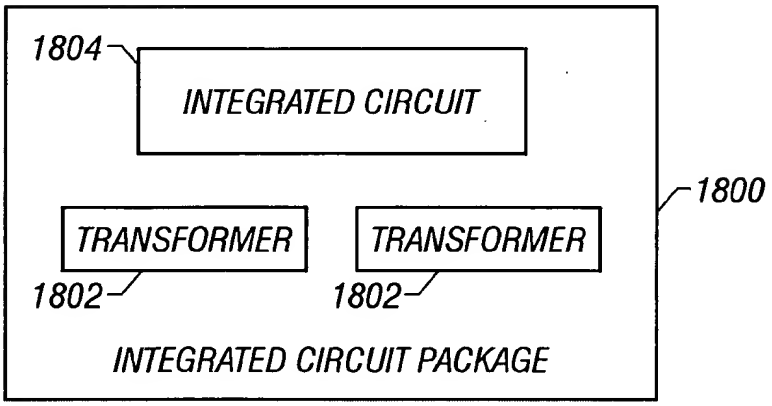

1804
INTEGRATED CIRCUIT
1800
TRANSFORMER
TRANSFORMER
1802
1802
INTEGRATED CIRCUIT PACKAGE

FIG. 18